PIC16F54 (base line 12bit) instructions

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Clear Watchdog timer	CLRWDT	004
Set Option Register	OPTION	002
Enter Seep Mode	SLEEP	003
Set Data Direction for PORT	TRIS PORT	00[PORT]
No Operation	NOP	000

CALL Subroutine CALL nn 9[nn] where nn is an 8

bit address

Jump to location GOTO nnn A[nn] or

B[nn] depending on high bit of address

Literal Operations

AND Literal with Working	ANDLW	E[nn]
OR Literal with Working	IORLW	D[nn]
Move Literal to Working	MOVLW	C[nn]
Return with Literal in Working	RETLW	8[nn]
Exclusive OR Literal with Working	XORLW	F[nn]

Logical Operations

_0g.0a.		
Add Working to File	ADDWF file, destination	1C0 + file (+ 20)*
AND Working with File	ANDWF file, destination	140 + file (+20)
Clear File	CLRF file	060 + file
Clear Working Register	CLRW	040
Compliment File	COMF file, destination	240 + file (+20)
Decrement File	DECF file, destination	0C0 +file (+20)
Decrement File Skip Zero	DECFZ file, destination	2C0 +file (+20)
Increment File	INCF file, destination	280 +file (+20)
Increment File Skip Zero	INCFSZ file, destination	3C0 +file (+20)
OR Working with File	IORWF file, destination	100 +file (+20)
Move Working to File	MOVWF file	020 +file
Move File	MOVF file, destination	200 +file (+20)
Rotate File Left through Carry	RLF file,destination	340 +file (+20)
Rotate File Right through Carry	RRF file,destination	300 +file (+20)
Subtract Working from File	SUBWF file, destination	080 +file (+20)
Swap high and low nybbles of File	SWAPF file, destination	380 +file (+20)
Exclusive Or Working with File	XORWF file, destination	180 +file (+20)

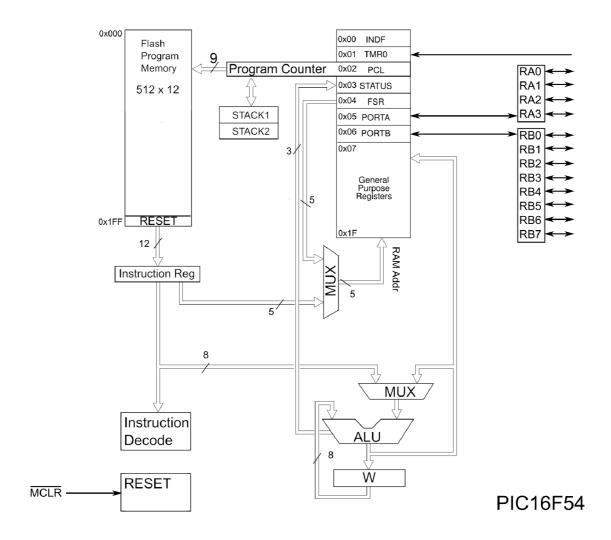
^{*}Note if result stored in file add 0x20 to op-code.

Bit Operations

Clear Bit in File	BCF file,bit	400 +file +bit*0x20
Set Bit in File	BSF file,bit	500 +file +bit*0x20
Test for Bit set in File	BTFSS file,bit	700 +file +bit*0x20
Test for Bit clear in File	BTFSC file,bit	600 +file +bit*0x20

The STATUS (0x03) register, which contains the zero and carry flags has the following bits:

7	6	5	4	3	2	1	0
PA2	PA1	PA0	TO	PD	Z	DC	C



PDIP, SOIC

